Claims

[c1]   1.An FDTD acceleration system for use with a host com-

puter operating FDTD software, comprising:

(a)a circuit comprising a plurality of one-dimensional

bit-serial FDTD cells;

(b)means for interfacing with a host computer data bus;

and

(c)means for accepting software calls from the host com-

puter.

[c2]   2.An FDTD acceleration system for use with a host com-

puter operating FDTD software comprising:

(a)hardware circuit means for calculating FDTD and PML

update equations;

(b)means for interfacing with a host computer data bus;

and

(c)means for accepting software calls from the host com-

puter.

[c3]   3.The system of claim 2 further comprising a memory

and a memory manager for temporarily storing data for

use by the hardware circuit means.

[c4]   4.A method of accelerating an FDTD simulation compris-

ing the steps of:

(a)offloading FDTD update equation to a hardware circuit comprising a plurality of one-dimensional bit-serial FDTD cells;

(b)accepting the updated values from the hardware circuit; and

[c5]   5.The method of claim 4 comprising the further step of temporarily storing updated equation data in a memory operatively connected to the hardware circuit.